CS 250 Spring 2017 - Lab 02

Due in lab Jan. 31 through Feb. 03, 2017

Submit your typewritten file in PDF format to Blackboard

**In-Lab Experiments, Part 1**

1. [5 points] As you turn the potentiometer knob to move terminal 2 from terminal 1 (connected to the 470 ohm resistor) towards terminal 3 (connected to ground), the Analog Input voltage linearly changes from 5 volts to 0 volts. Carefully observe Red LED1 and Red LED2. Describe the behavior of the two LEDs with respect to the action of the potentiometer.
2. [15 points] Plot your data point pairs (NAND1 input voltage from potentiometer, NAND1 output voltage). Comment on the shape of the function NAND1 output voltage = f(NAND1 input voltage from potentiometer) displayed in your plot. Does f show digital behavior?
3. [10 points] NAND1 produces a high quality (more digital) output signal despite the many poor quality logic 0 and logic 1 voltages and voltages within the gap between the valid logic levels that the potentiometer voltage provides to NAND1. Why is the behavior of NAND1 to a poor quality input so important to computer circuits comprised of billions of transistors?

**In-Lab Experiments, Part 2**

1. [10 points] Fill in the following table with your observations from Part 2 experiments.

|  |  |
| --- | --- |
| Clock source | Typical number of bounces observed from LEDs A, B, C, D (74163 output) |
| Clock 1 (potentiometer) |  |
| Clock 2 (SPST switch) |  |
| Clock 3 (SPDT switch) |  |
| Clock 4 or 5 (SR Q or Q’) |  |

**Take Home Questions**

1. [10 points] Why is skipping consecutive numbers in the output of the 74163 counter an indication of switch bounce?
2. [10 points] If the 74163 advances the count by 1 for a single Clock 3 input this means that the switch did not bounce that time. True or False? Explain your answer.
3. [10 points] What is the mathematical expression for the number of bounces observed by the 74163 chip circuitry as contrasted with the number of bounces that your eyes are capable or observing by examining the 74163 output using LEDs A, B, C, and D?
4. [10 points] How does the memory capability of the SR latch (NAND2 and NAND3) transform the bouncing SPDT switch input into a bounce-free output?
5. [20 points, 5 points each of the four parts] Design a logic circuit to compute the function F(A,B,C) = 1 when at least two of the A, B, and C inputs are logic value 1. Show the following for F(A,B,C): (1) truth table, (2) K-Map, (3) minimized Boolean expressions in both SOP and POS form, (4) draw schematics for both the SOP and POS expressions using NAND and NOR gates, respectively.